2nd Sem D.E

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12EC077

M.Tech. Degree Examination, June / July 2014
Synthesis and Optimization of Digital Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Draw the Y chart for different level of abstractiona dn synthesis. Explain different levels briefly. **(10 Marks)**

b. Explain the characteristic numbers of a graph and find whether the graph shown in Fig. Q1 (b) is perfect graph or not. **(10 Marks)**

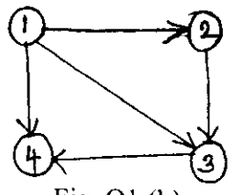

Fig. Q1 (b)

2 a. Consider the function $f = a'b + b'c + ac'$. Compute the boolean difference, consensus and smoothing with repsect to variable a. Also indicate them in cubical form. **(10 Marks)**

b. Define the following with respect to concept of graph theory and give an example for each:
i) Directed graph.
ii) Hypergraph. **(04 Marks)**

c. Draw OBDD and then ROBDD for the function f=(a+b)c with variable order a, b, c. **(06 Marks)**

3 a. Give the behavioral representation of Full Adder in VHDL. **(06 Marks)**

b. Explain the structural representation for an abstract model and for the given model in Fig. Q3 (b), find hypergraph, module-net incidence matrix and bipartite graph. **(06 Marks)**

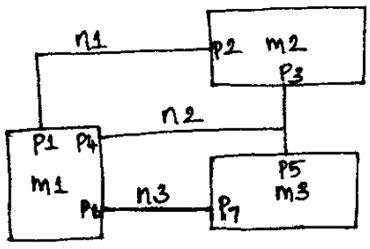

Fig. Q3 (b)

c. Explain tree height reduction optimization. For the given arithmetic assignment statement $x = a * (b * c * d + e)$ draw the reduced parse tree and compute the reduced tree height along with total number of operations. **(08 Marks)**

4 a. Consider a three input, two output function $f = \begin{bmatrix} f_1 \\ f_2 \end{bmatrix}$

where $f_1 = a'b'c' + a'b'c + ab'c + abc + abc'$, $f_2 = a'b'c + ab'c$

Find its minimum cover, irreduntant cover and minimal cover with respect to single implicant containment. Represent the same using three dimensional boolean cubes. **(12 Marks)**

b. Represent the function, $f = ab + ac + ab'c' + a'$ in positional cube notation and check if it is a tautology. **(08 Marks)**

5 a. Explain briefly heuristic minimization operators expand, reduce, reshape and irreduntant. **(04 Marks)**

b. Consider the function, $f = a'b'c' + ab'c' + a'bc' + a'b'c$ with abc' as don't care condition form an expanded cover. **(06 Marks)**

c. For the finite state machine in Fig. Q5 (c), obtain the minimum state diagram. **(10 Marks)**

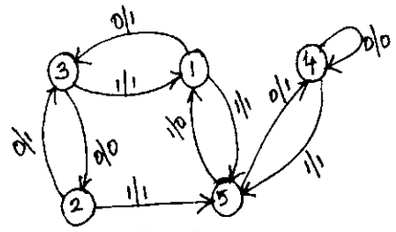

Fig. Q5 (c)

6 a. Compute kernels and co-kernels based on matrix representation for $f_x = ace + bce + de + g$. **(08 Marks)**

b. Write pseudocode for ALAP scheduling algorithm. Also for the given model fragment:

$x/ = x + dx$

$u/ = u - (3 * x * u * dx) - (3 * y * dx)$

$y/ = y + u * dx;$

$c = x/ < a$

Draw ALAP schedule under latency constraints of 4 steps. Assume unit execution delay for all operations. **(12 Marks)**

7 a. A logic network with primary input variables {a, b, c, d, e} and primary output variables {w, x, y, z} is described by the following equations:

$p = ce + de$; $q = a + b$; $r = p + a'$; $s = r + b'$; $t = ac + ad + bc + bd + e$; $u = q'c + qc' + qc$;

$v = a'd + bd + c'd + ae'$; $w = v$; $x = s$; $y = t$; $z = u$;

i) Draw the corresponding logic network and logic network graph.

ii) Perform elimination, extraction and substitution transformations for the logic network with appropriate examples. Show the transformed network. **(12 Marks)**

b. Briefly explain Hu's scheduling algorithm with pseudocode. **(08 Marks)**

8 Write short notes on:

a. ATPG.

b. Antifuse based FPGA.

c. Loop folding.

d. LEFT-edge algorithm. **(20 Marks)**

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